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**Special Issue on Selected Papers from
the *Engineering and Applications* Track of the
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Algorithms (ESA 2004)*
Guest Editor's Foreword**

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This issue of *Journal of Graph Algorithms and Applications* includes full journal versions of three papers selected from the papers presented in the *Engineering and Applications* track of the *12th Annual European Symposium on Algorithms (ESA 2004)* held in Bergen, Norway, September 15–17, 2004. These contributions were invited for publication based on their high merit and relevance to *JGAA*. They all have gone through the standard refereeing process of *JGAA* to ensure high publication standards.

The paper *Contraction and Treewidth Lower Bounds* by Hans L. Bodlaender, Arie M. C. A. Koster and Thomas Wolle is a very thorough investigation of obtaining lower bounds for the treewidth of a graph by considering its minors. The authors show complexity results related to this approach and propose a number of new heuristics. They evaluate the performance of their heuristics by comparing them with other methods in an extensive set of experiments.

In the paper *Distributing Unit Size Workload Packages in Heterogeneous Networks* Robert Elsässer, Burkhard Monien and Stefan Schamberger consider the problem of distributing indivisible tokens, representing units of load, evenly among the nodes of a heterogeneous network. They show that a randomized strategy based on random walks of tokens effectively minimizes the maximal overload of a node. They also present experimental results which indicate that their method may actually be faster in practice than the theoretical bounds would predict.

The paper *Finding Dominators in Practice* by Loukas Georgiadis, Robert E. Tarjan and Renato F. Werneck is concerned with developing fast implementations for the problem of computing the domination relation on the nodes of a directed root graph. This problem arises, for example, in the analysis of the control structure of a program for the purpose of generating an optimized code. The authors consider and compare experimentally a number of methods, including the theoretically fastest ones, and discuss implementation issues which were important in obtaining fast codes. They used in their experiments control-flow graphs produced by compilers and graphs representing VLSI circuits.